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Minimization of Leakage Power of 1-bit Full Adder in 180nm CMOS Technology

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ABSTRACT: In designing of digital signal processors, image processing, microprocessors full adder is the main requirement in VLSI design. Today, full adder design with better performance, high speed, less area with less delay is is one of the main challenges for VLSI engineers. This paper proposes 1-bit full adder using stacking effect. This proposed full adder has been simulated using 180nm CMOS process technology at 1.8V supply voltage using Cadence virtuoso. The results of the proposed full adder have been compared with results of conventional full adder. The result analysis shows that the proposed adder circuit is efficient in terms of static power dissipation as compared with conventional adder circuit.

KEYWORDS: Static Power Dissipation, CMOS, 180nm Technology, Full Adder, Leakage current, Power analysis.

I.INTRODUCTION

The performance of VLSI systems are measured in terms of speed, area, delay, power consumption and cost. There are two main reasons to reduce the power consumption of a circuit. First one is, increase the battery life to save energy of battery operated systems. Second one is, increase of density function which is implemented on single IC, by reducing the power consumption[2].

There are different logic styles having its own advantages and disadvantages was proposed to implement speed of 1 bit full adder. Addition is the universal operation which is utilised in tasks like division, multiplication, subtraction etc. It is very important to choose the adder design which gives the better performance of digital systems. The power consumption is mainly divided into three major components namely switching power, short circuit power and static power.

1. Switching power: It is the power dissipated by the system while switching of transistors from HIGH to LOW or LOW to HIGH which results in terms of charging and discharging of load capacitances.
2. Short-circuit power: It is the power dissipated when the transistor is in switching mode, here the current flows from power supply to ground.
3. Static power: It is the power dissipated when the transistor is in OFF state. It is independent of input. No matter whatever the input is applied.

Switching power and short-circuit power indicates the dynamic power consumption. Dynamic power denotes overall power in CMOS circuits. It is represented as shown in equation (1)

$$P_{dynamic} = C_L . F_{clk} . V_{DD}^2 \quad (1)$$

C_L is load capacitance, V_{DD} is power supply voltage, f_{clk} is system clock frequency

$P_{dynamic}$ is the power when the load capacitance charges and discharges. When the transistor switches dynamic power dissipates and during no switching there is no power dissipation. Dynamic power totally depends on clock signal of input signal applied[1]. It is given as

$$P_{avg} = P_{switching} + P_{short\_ckt} + P_{leakage} + P_{static} \quad (2)$$

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The arrangement of this paper is as follows. Section II talks about related previous designs of full adder circuit. Section III describes the proposed full adder circuit with stacking effect. In section IV the simulation results of proposed technique and the comparison of proposed results with the conventional design is presented. Conclusion of this work has been given in section V.

II.PREVIOUS WORK

In sleep transistor technique two extra transistors called sleep transistors are placed between Vdd & pull up network and ground and pull down network. Sleep transistors are made turn off when the circuit is not in use. This reduces the leakage power during stand by mode[4,5].

In lector technique two extra transistors i.e one NMOS and one PMOS transistors are placed between pull up and pull down network in series in each CMOS gate. The resistance path from Vdd to ground is increased in order to minimize the leakage current[6]. This technique works effectively for the circuit in both active and stand by mode[7].

In drain gating technique extra sleep transistors are inserted between pull up and pull down networks. One PMOS sleep transistor is placed between pull down and ground network[8]. During active state both transistors will turn on by increasing the resistance of conducting path and reduces the leakage current[6].

In zigzag approach for two circuits sleep transistor is used alternatively. At the first stage pull down transistor is used. At the second stage pull up transistor is used[9]. This zigzag method reduces the leakage current.

III.PROPOSED TECHNIQUE

A. Full Adder Design

Full adder performs addition operation with three bits of inputs and gives 1 bit of two outputs namely sum and carry. The truth table of full adder is shown in the figure 1. A,B,C are the binary inputs and sum, carry are the outputs. The expression for sum and carry are given as below.

$$Sum = A \hat{} B \hat{} C \quad (5)$$

$$Carry = AB|BC|AC \quad (6)$$

Table 1: Truth table of 1-bit full adder

A	*B*	*Carry-In*	*Sum*	*Carry-Out*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The basic schematic diagram of 1 bit full adder is represented as shown in figure in transistor level.

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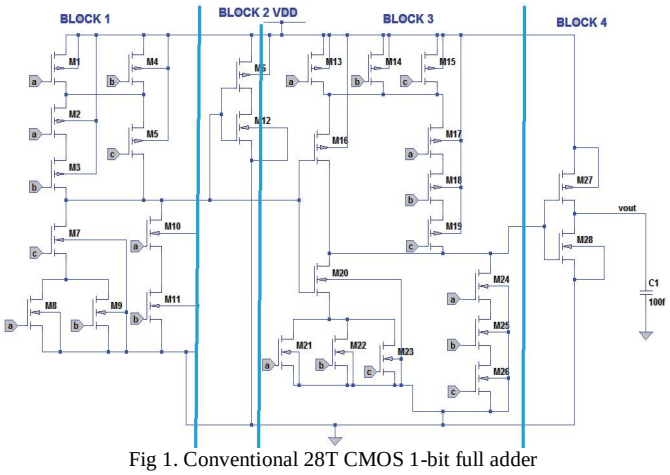

Fig 1. Conventional 28T CMOS 1-bit full adder

Figure 1 represents the basic full adder schematic diagram at transistor level. It is designed with basic equations of sum and carry using NAND and NOR gates as they are the universal gates of digital design.

B. Technique

A parallel combination of one NMOS transistor and one capacitor is connected in series between pull down network and ground as shown in the figure 2.

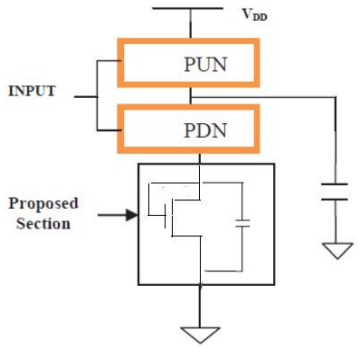

Fig 2. Block diagram of proposed technique

In this technique the drain of NMOS transistor is connected to the gate terminal of itself by self controlling the ON-OFF conditions. Low Vth transistors are used in order to get desired output swing. By adding one extra NMOS transistor the resistance of conducting path increases. Capacitor is inserted because of its high reactance property towards DC signal. Once the capacitor charges upto VDD then it will remain at the same state and blocks the further leakage current.

Case A:

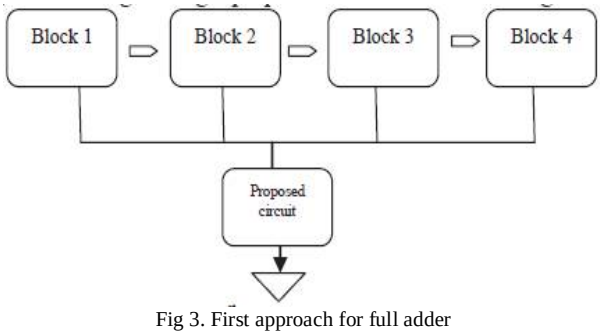

Fig 3. First approach for full adder

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As shown in the figure 3, all four blocks are grouped together and connected to a proposed circuit hence the delay time will increment and power consumption is reduced as we have utilized less number of transistors.

I. Case B:

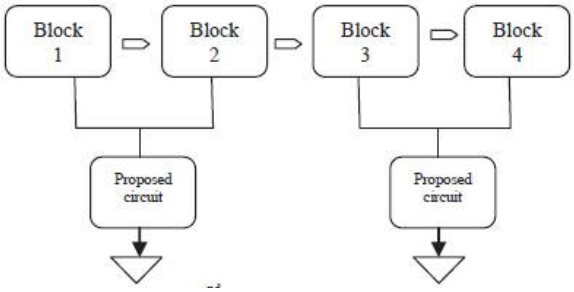

Fig 4. Second approach for full adder

As shown in the figure 4, each two-two blocks are grouped together and connected to proposed circuits respectively hence the delay time will be minimized and power consumption will increase as compared to the Case A as we have increased the number of transistors in the proposed section

II. Case C:

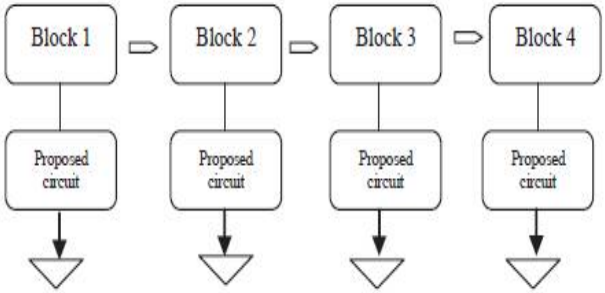

Fig 5. Third approach for full adder

As shown in the figure 5, each individual blocks are connected to one-one proposed circuits respectively hence the delay time will be decremented and power consumption will be incremented because we have incremented the number of transistors in proposed section.

V. RESULTS AND DISCUSSION

The figure 6. is the schematic diagram for the conventional full adder circuit. It is simulated in the both 180nm technology using Cadence Virtuoso at 1.8V supply voltage input and at 1.8V DC input.

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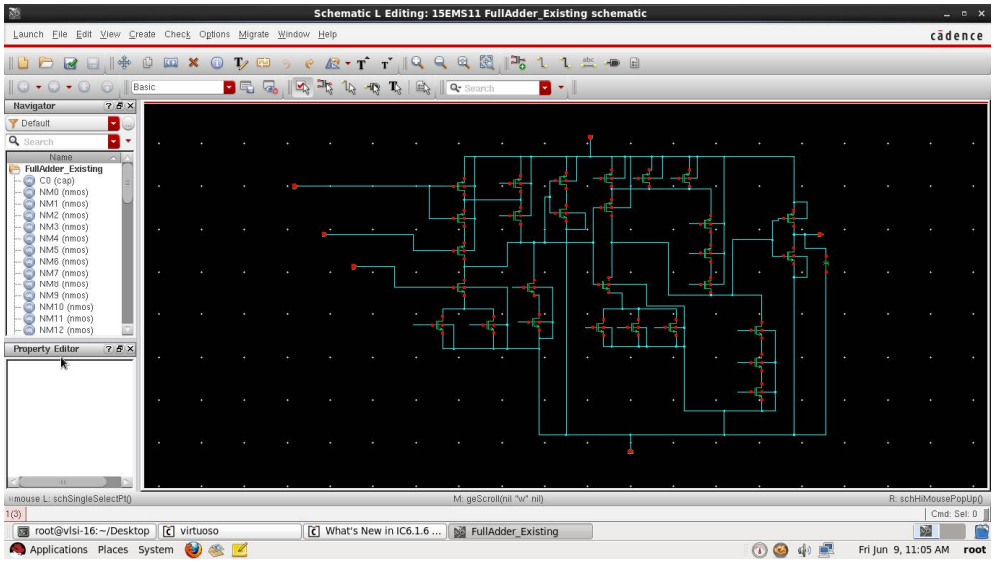

Fig 6. Schematic of conventional 1-bit full adder

The figure 7. is the schematic diagram for the proposed section of full adder circuit which is shown in the Case A. It is simulated in the 180nm technology Cadence Virtuoso.

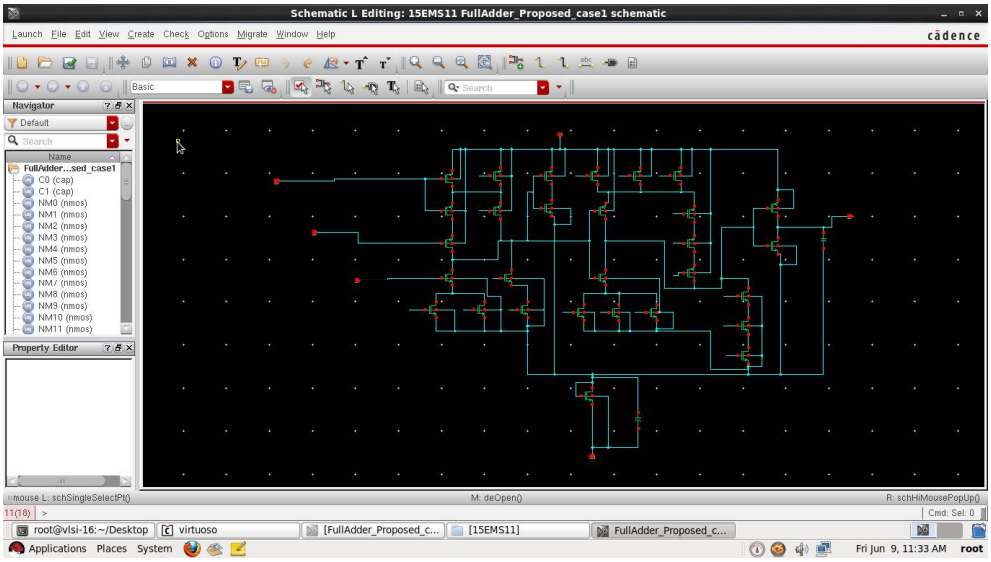

Fig 7. Schematic of 1-bit full adder for case A

The figure 8. is the schematic diagram for the proposed section of full adder circuit which is shown in the Case B. It is simulated in the both 180nm and technology Cadence Virtuoso at 1.8V input supply voltage and at 1.8V input DC voltage.

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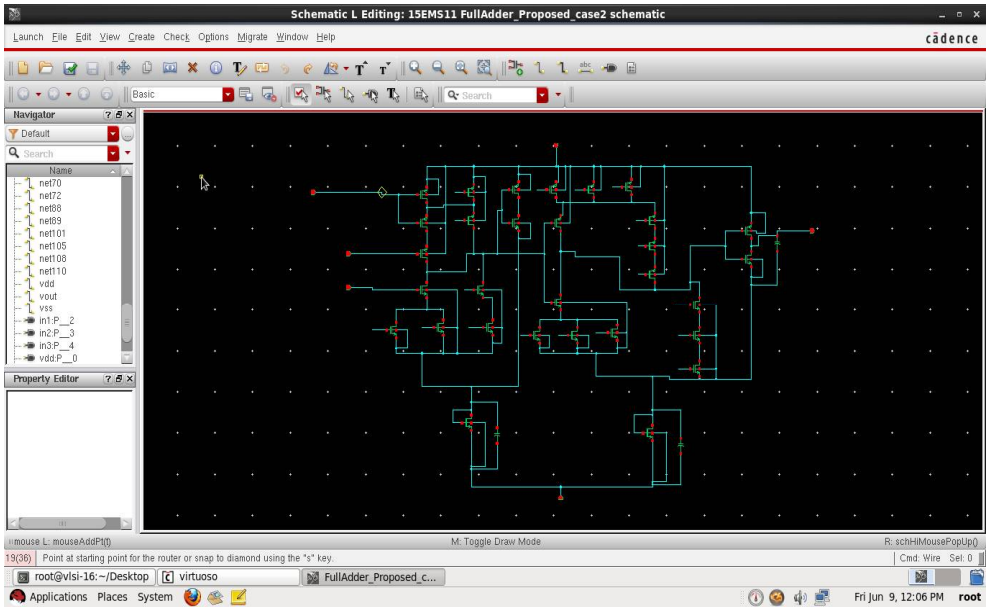

Fig 8. Schematic of 1-bit full adder for case B

The figure 9. is the schematic diagram for the proposed section of full adder circuit which is shown in the Case C. It is simulated in the 180nm technology Cadence Virtuoso at 1.8V input supply voltage and at 1.8V input DC voltage.

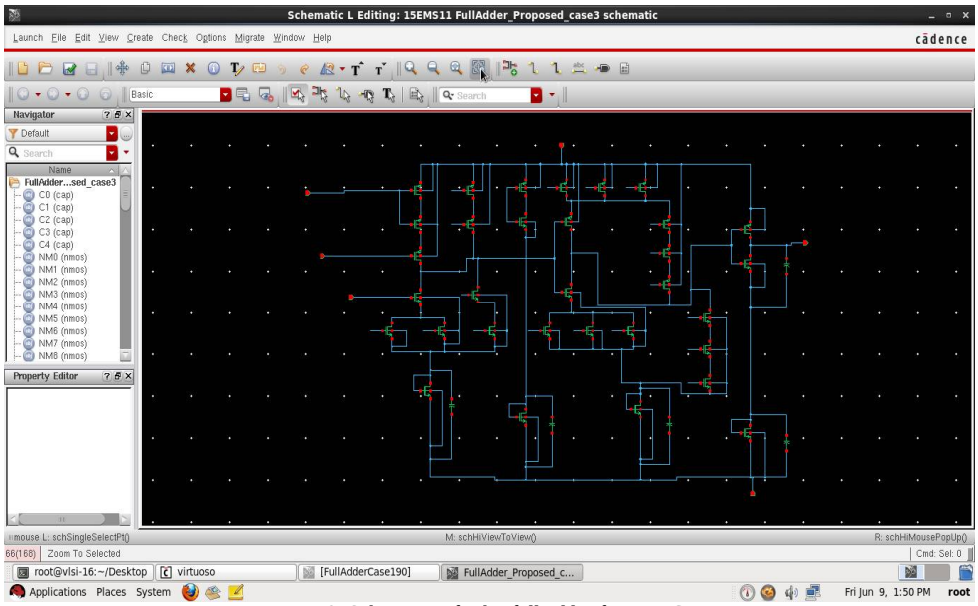

Fig 9. Schematic of 1-bit full adder for case C

The below figure 10. shows the output of the full adder circuit which is simulated in the both 180nm technology Cadence Virtuoso. Here A,B and Cin are the inputs and Sum and Cout are the outputs.

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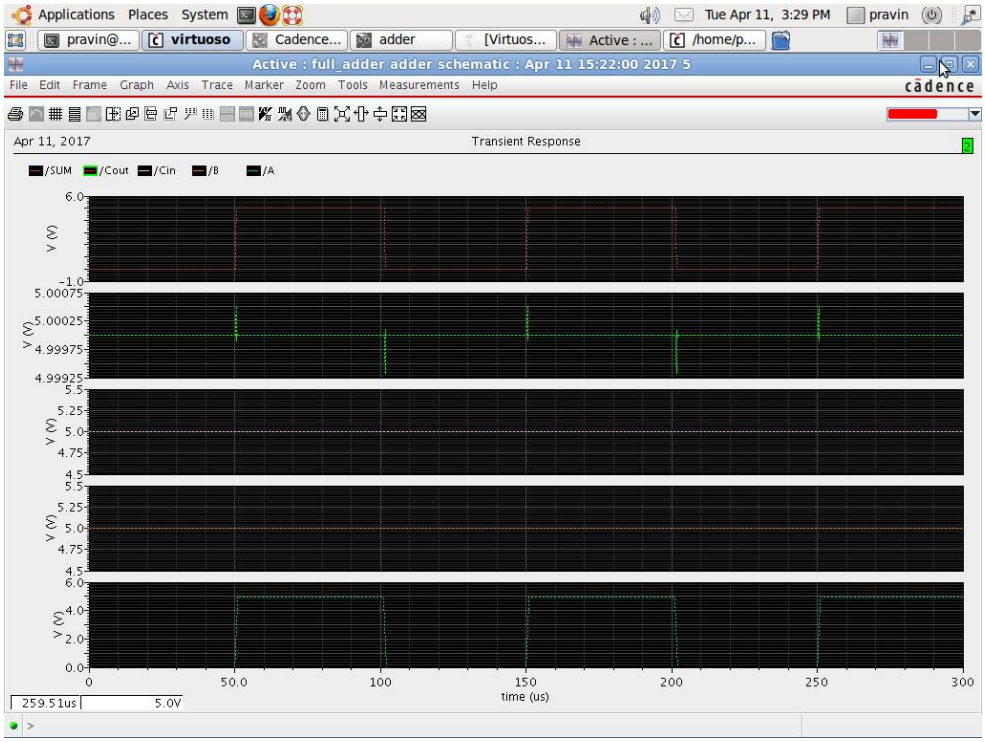

Fig 10. Output waveform of 1-bit full adder

Table 2 indicates the comparison results of conventional adder and proposed adders in three cases. It is clearly shown that the power dissipation is decreased in all three proposed sections as compared to conventional adder. And the power dissipation has increased as the technology increases.

Table 2: Comparative Results of Leakage Power

Static Power Dissipation (Leakage power)	
Case Study	**180nm Technology**
Conventional	109.1566pw
Proposed case 1	76.847pw
Proposed case 2	77.575pw
Proposed case 3	77.70pw

VI.CONCLUSION

Leakage power dissipation has increased due to scaling down the device size and threshold voltage. To reduce the standby leakage current a new stacking technique is proposed for 1 bit full adder circuit. This proposed circuit increases the resistance of conducting path from pull down network to ground terminal during stand by condition. The proposed section is applied to full adder and analysed with three different cases. We have observed that all three proposed full adders performs better than the conventional full adder by reducing the leakage power. The simulation is carried out at 1.8V supply voltage in 180nm CMOS technology using Cadence virtuoso. In future the proposed full adder can be implemented using 90nm and 45nm technologies and proposed full adder can be used in applications like Wallace Tree Multiplier, Arithmetic Logic Unit, Flas Analog to Digital circuit etc for better performance.

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